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Design Quality Closure: Enabling Less Iteration at Every Handover in a Design Process

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System-on-chip (SOC) designers and mask shop engineers have something in common: The quality of what they deliver can only be as good as what they get from the teams before them. For example, SOC designers expect developers of intellectual property (IP) to deliver blocks that are ready for smooth integration, and mask shop engineers expect back-end designers to deliver graphic design system (GDS) data that is design for mask manufacturing (DFMM)-aware.

SOC designers and mask shop engineers see their common challenge (i.e., expecting the most out of their respective predecessors) from different perspectives: While significant effort is put into defining quality standards for IP, little formalism is available to those interested in breaking down the wall between design houses and mask shops. However, regardless of where they stand in the design chain, engineering and product managers now spend between 20 and 40 percent of their time tracking the design quality metrics that they consider critical. This time could be dramatically reduced with a more formal understanding of what constitutes design quality and with an easier way for designers to check quality run after run.

More specifically, at the DFMM level, stopping any mask during mask processing, which requires a waiver from the customer, will add a delay of between 12 and 24 hours to its delivery schedule depending on the stage during which the problem is detected. In the worst case, the mask will pass normal inspection, allowing a too well-defined, repeated defect to kill the wafer, when this defect could have been anticipated. Since such quality issues are usually discovered very late in the entire process, up to final circuit testing before packaging, they can often delay the entire project by a month or more.

A methodology for resolving these issues is through design quality closure (DQC), which can be defined as the condition of passing an acceptable subset of predefined quality checks for safe handover to the next engineering team. This, of course, requires a set of predefined quality checks (also known as methodology rules, guidelines or best practices) with which designers must comply, as well as a configurable DQC tool to monitor and report compliance. Closure happens when the designer is sufficiently confident that all critical parameters are met, so that his design work can be carried out to the next phase, without putting the chip objectives (function, area, timing, power, manufacturability, testability, etc.) at risk.

Quality metrics exist to some extent, but have, until recently, been rules that must be tracked manually. The Quality of Electronic and Software Intellectual Property (QIP) metric standard, for instance, allows companies to evaluate IP from internal groups or third parties. However, since it is based on Excel spreadsheets, it adds another layer of labor to designers' loads. DQC is more useful if applied automatically to all steps of a chip design process. DQC characteristics include reuse of quality standards when available, openness to user specifics (design flow, know-how, etc.), and opportunity to formalize and deploy new quality rules over time.

Design, mask making and process engineering have always seen themselves as separate areas that seem to depend on sets of rules that isolate them from having to understand one another's technology. However, the ever-increasing number and complexity of these design rules is making the traditional isolated design paradigm unsupportable. Today, close interaction between manufacturing, mask and design communities is key to successful product development.

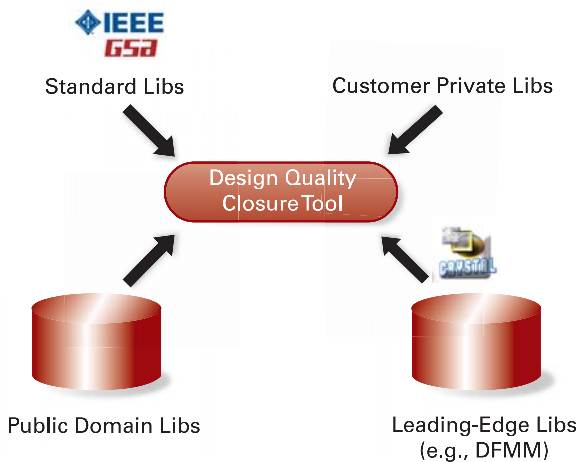
An Optimized DQC Tool

A key aspect of DQC is to incorporate quality checks throughout the entire design flow. A DQC tool allows a designer to take advantage of an existing design flow, synthesize all electronic design automation (EDA) artifacts into easy-to-read dashboards and make design decisions on the basis of factual design data. By automatically generating quality reports, such a tool can save weeks of time. The DQC tool tracks and captures all parameters and objects affecting design quality from multiple sources throughout the IP or SOC design and integration lifecycle, and offers "checklist-driven" design assistance to help users monitor specifications, coding, integration, front-end/back-end implementation, verification and all other relevant tasks.

Ideally, a DQC tool implements a three-phase approach. First, it helps companies set up their design methodologies by importing hundreds of pre-written design quality checks easily. Second, it automates the quality checks. Finally, it supports the methodology deployment to all involved design teams with automatically filled dashboards and quality closure reports.

For maximum flexibility and utility, such a DQC tool would allow the designer to import design quality checks by using one of the available libraries or by creating a unique library in a few hours (Figure 1). It would then configure and automate dashboards by editing software sensors that link the quality checks to the current design and verification flow, and permit DQC monitoring by deploying the dashboards and issuing quality reports on-the-fly.

Figure 1



A DQC tool allows for the integration of libraries from multiple sources.

The functioning of such a tool is most optimum when it provides non-intrusive assistance to the designer. This capability is exemplified by dashboards that complete themselves automatically, on the basis of the latest information found in the customer flow, and that reflect the set of quality items that designers need to monitor. The dashboards must address the most critical areas of design quality and design reuse: specifications, architecture, front-end design, back-end design, verification, IP packaging, software development and overall project management. In addition, they should be generated on-the-fly from customer flow outputs. They should be available in different forms (single IP, multi-core design, etc.) and always be up-to-date, by construction. This allows fact-based quality closure monitoring by project managers, and complements the other mechanisms that managers have for tracking resources and schedules, making a major contribution to timely and accurate quality closure.

Applying DQC to DFMM

Such industry initiatives as the European CRYSTAL[1] collaborative research and development (R&D) program are intended to significantly improve DFMM by identifying and formalizing recommended design practices to make mask manufacturing a more efficient and less-iterative process. The goal is to help improve design consistency, on-time delivery and the cost of photomask design by providing access to real data about (1) the manufacturing challenges at mask shops and (2) the design practices in the upstream design phases that would solve these challenges. Such initiatives would also align the development and availability of the real-time data points to the need for leading-edge design libraries in addition to the standard libraries.

Specific mask-level issues that need to be addressed in the manufacturing process include:

- Grid mismatch between design and fractured data. This generally causes micro gaps and shape border offsets.
- Sub-geometries created during optical proximity correction (OPC) application, which will generate mask inspection issues.
- Metal layer filling with "wild" cutting, which generates acute angles and sub-geometries.
- Multi-project wafers with exceeded process tolerance window when several designs are assembled.

A DQC tool that uses real manufacturing data can highlight these issues before it is too late. For example, it can check possible grid mismatch by snapping between the design and desired fractured data, and by analyzing the fracturing log report for on-grid geometries. It can also check the number of sub-geometries smaller than the minimum feature size after the OPC application step and the number or acute angles after the metal layer filling step.

This type of design test usually exists at a different level of data generation, but never compares results to the mask process requirements, the type of mask process which will be used being unknown by the designers. In addition, the set of rules that will be used for final mask manufacturing are not introduced early enough in the design flow to be captured in the first design quality checks.

Applying DQC to Design for Reuse

It is generally accepted that reusing semiconductor IP blocks in a core-based design strategy is the most suitable response to the stringent constraints involved in SOC design. The principal challenges for design for reuse can be summarized as follows:

- The quality of an IP block is defined by its ability to be integrated safely into an SOC, which involves careful management of various engineering practices throughout the block life cycle.
- For large semiconductor companies, implementing a quality-based strategy to reuse IP blocks is one of the strategic targets to reduce the costs, risks and design timelines of complex ICs.
- For IP vendors, it is absolutely vital to produce the highest quality IP possible and to be able to document that quality for prospective customers.
- For an SOC project leader with several IP sources available, a highly sensitive question is "How can I qualify the available IP blocks to minimize risk at chip integration?"

Designers and integrators of reusable blocks cannot meet their objectives merely by using the most up-to-date EDA software along with design guidelines too loose or too general to really make a difference. It is absolutely crucial that design guidelines (whether stipulated by manufacturers or public literature) be applied on a daily basis by all teams involved in block development. Each engineer, whatever his or her involvement in the project, must be able to identify and assess the quality requirements relating to his or her particular activity.

Among the most essential issues that must be considered to guarantee the success of a design-for-reuse strategy are:

- Enforcing design-for-reuse practices. Once defined at a corporate level, stable design-for-reuse practices should be enforced through design teams without incurring unwanted engineering overhead.
- Managing design dynamics. Changing specifications and test cases are part of real-life designs, and should be dealt with efficiently. Instead of relying on hard copies or Excel spreadsheets that are time-consuming and error-prone, and that eventually become obsolete, design documents should be issued automatically from the design environment with up-to-date information.
- Ensuring stable design-for-reuse criteria. Large semiconductor corporations usually find added productivity in homogenizing their design flows through teams. However, even standardized

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design flows evolve constantly with added capabilities, new needs to inter-operate with customers and partners, etc. Benefits result from insulating design-for-reuse criteria monitoring from the multiple and changing EDA tools, file formats and databases.

Example of DQC Deployment at STMicroelectronics

Within the home entertainment and display (HED) group of STMicroelectronics, quality standards for internally developed synthesizable IP have been in place for more than 10 years, culminating in automation of the full design flow, from register transfer level (RTL) to front-end package. However, although this automated flow has proven its value by shortening design times and enforcing design standards, the 20+ computer-aided design (CAD) tools used produce hundreds of logs and reports, which take a significant amount of time to check for errors or deviations. An effort was therefore launched to find a way to automatically extract quality metrics from the set of logs and reports produced by the flow. In addition to speeding up data review, the solution also had to allow the computed metrics to be published once the IP was delivered, and possibly enable consolidation with metrics from other IP to compute SOC quality metrics.

A DQC tool was identified that uses "sensors" working on different sources to capture complex information from log files and extract quality metrics. This data was released to a Web-based central database, where released metrics were compared with local "ready-to-release" metrics. Metrics could be compared across several releases, and reviewed and published in the form of dashboards.

A third-party DQC tool was recently used by STMicroelectronics' HED group to improve IP quality in an SOC with more than 80 IP blocks. The DQC tool extracted key data from the HED IP design flow to allow for monitoring in detail of the quality of IP during its development cycle, to automatically produce IP integration documents at delivery time, and to consolidate IP quality metrics for the given set of IP present in the SOC. This approach led to improved IP quality and reduced time to integration.

STMicroelectronics' HED group formalized 110 quality checks and design metrics by consensus among designers, tool specialists and methodology experts. Then, using the DQC tool, it developed 205 relevant sensors for data capture from about 140 design flow artifacts (Figure 2), and wrote formulae for data combination and shaping. With those in place, extracting the metrics and creating the IP integration document with the DQC tool takes less than five minutes. The automatic generation of the IP integration document saves one day per IP iteration and lowers the risk of subjective interpretation.

Figure 2

An optimized DQC tool uses factual data from the design flow and allows for on-going monitoring of quality checks and metrics.

Through the DQC tool Web interface, different stakeholders (IP designers, IP managers, CAD, SOC integrators, etc.) are able to share and review metrics in real time, see history and compare multiple IP. This allows IP designers to continuously measure their compliance with the set of recommended quality criteria, without overhead, and immediately discover errors and deviations.

Communication between IP providers and integrators is fact-based, formalized and instantaneous, and the CAD team and methodology experts can easily maintain and update the set of quality metrics and sensors with an immediate deployment and adoption via the Intranet.

Conclusion

It is well known that added design productivity comes with streamlining the design flows and processes that semiconductor companies have in place. This, in turn, requires the documentation and implementation of robust handover procedures between engineering teams that follow each other sequentially. Two real life examples are (1) the need for IP designers to measure their deliveries with respect to quality criteria that make a positive impact on SOC integration and (2) the need for SOC back-end designers to prevent mask manufacturability issues by adopting DFMM-specific practices.

A formalized strategy for DQC, with associated monitoring tool and dedicated quality check libraries, is of major help for facilitating and strengthening handovers. It helps designers to deliver work in complete awareness of what the next team in the design process is expecting from them.

Such a strategy covers the needs of those design teams using standard quality checks and metrics (e.g., QIP for IP design practices), and supports the definition and deployment of proprietary practices when no standard is available (e.g., DFMM).

To all it brings added design quality, productivity and predictability; and this makes DQC a must-have capability in today's design environments. ■

About the Author

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References

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