

Enabling IP Quality Closure at STMicroelectronics with VIP Lane

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PROJECT OBJECTIVES

1. Formalize the quality checks & design metrics by consensus among designers, design managers & CAD group
2. Define “**IP Quality Closure**” as the condition of passing an acceptable subset of predefined quality checks
3. Monitor the IP quality more efficiently & make no compromise on the Time to Quality Closure
4. Show **productivity improvements** at the levels of design teams (generating reports automatically, supporting design reviews) & CAD support team (deploying quality checks & metrics)

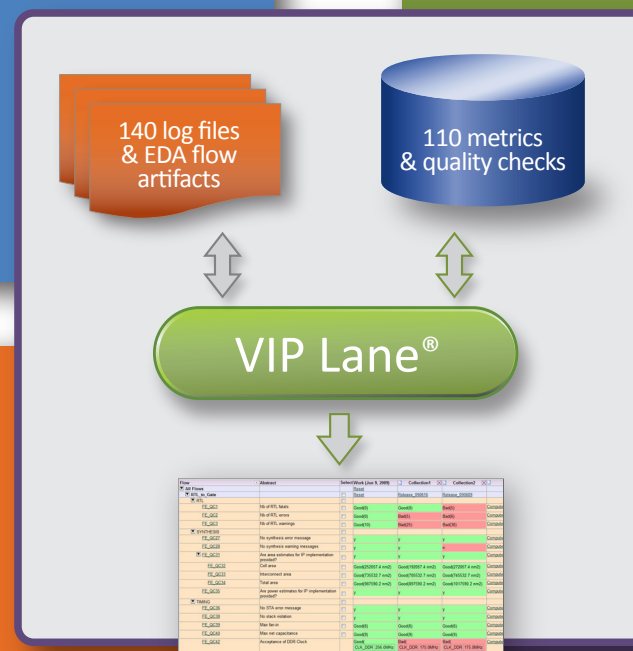
DELIVERABLES

Solution implemented with VIP Lane for a 55nm SoC Design

1. Library of 110 quality checks & design metrics, based on 205 sensors collecting data from 140 different sources
2. **Automated generation** of ST proprietary “IP Integration Document”
3. **Flexible reporting** with dashboards (IP latest status, IP release history, IP catalog at SoC level)

THE PROBLEM

1. ST designs SoC with 80+ IP blocks
2. Each IP block subject to several design iterations during SoC integration phase
3. **Need to implement & document IP quality** for effective integration & predictable results
4. ST uses an “IP Integration Document” with over 100 critical design metrics & quality checks
5. Designers have **no time** to issue a new IP Integration Document for each IP release (metrics hard to track; tedious, manual process)



BENEFITS

1. All metrics extracted & presented in dynamic dashboard in **less than 5 minutes**
2. Automated generation of IP Integration Document **saves ONE workday per IP release**
3. Closer collaboration between IP & SoC teams
4. Recommended practices, QC & design metrics more easily adopted by designers.
5. Approach **scalable** from frontend design practices to backend & software development

140 log files
& EDA flow
artifacts

110 metrics
& quality checks



VIP Lane®



Item	Abstract	Setup/Work (Jan 9, 2008)	Collection 1	Collection 2	Collection 3
W all Files		Start	Start	Start	Start
W all, in Case		Start	Start	Start	Start
W all		Start	Start	Start	Start
TEL_SG1	Top of RTL, Meta	Good(1)	Good(1)	Bad(1)	Complete
TEL_SG2	Top of RTL, errors	Good(1)	Good(1)	Bad(1)	Complete
TEL_SG3	Top of RTL, warnings	Good(1)	Bad(1)	Bad(1)	Complete
W 1/12/08		Good(1)	Bad(1)	Bad(1)	Complete
TEL_SG2	No synthesis error message	Y	Y	Y	Complete
TEL_SG3	No synthesis warning message	Y	Y	Y	Complete
TEL_SG1	Are error estimates for P-implementation present?	Y	Y	Y	Complete
TEL_SG2	Cell area	Good(20857 4 mcd)	Good(18857 4 mcd)	Good(17857 4 mcd)	Complete
TEL_SG3	Interconnect area	Good(73810 7 mcd)	Good(76810 7 mcd)	Good(74810 7 mcd)	Complete
TEL_SG1	Total area	Good(49119 2 mcd)	Good(49119 2 mcd)	Good(49119 2 mcd)	Complete
TEL_SG2	Are error estimates for P-implementation present?	Y	Y	Y	Complete
W 1/16/08		Good(1)	Good(1)	Good(1)	Complete
TEL_SG3	No STA error message	Y	Y	Y	Complete
TEL_SG1	No slack violation	Y	Y	Y	Complete
TEL_SG2	Max fanin	Good(1)	Good(1)	Good(1)	Complete
TEL_SG3	Max net capacitance	Good(1)	Good(1)	Good(1)	Complete
TEL_SG1	Acceptance of DSR Clock	Good	Bad	Bad	Complete
		CLK_200_100 (200 MHz)	CLK_200_100 (200 MHz)	CLK_200_100 (200 MHz)	
		CLK_100_100 (100 MHz)	CLK_100_100 (100 MHz)	CLK_100_100 (100 MHz)	
		CLK_100_50 (100 MHz)	CLK_100_50 (100 MHz)	CLK_100_50 (100 MHz)	