

Save weeks by generating **dashboards** and **quality reports automatically**

Why VIP Lane?

- Formalize your best design practices into repeatable quality checks and metrics
- Enable fact-based quality monitoring at no overhead to design teams and design management
- Save weeks on every design with automatically-generated compliance reports and highlighted exceptions
- Monitor worldwide projects with fact-based accountability
- Take advantage of your multi-vendor design and verification flow(s)
- Implement monitoring capabilities applicable to any design (digital, analog, software, IP , SoC or embedded system)
- Leverage your quality assurance legacy by reuse or integration of home-grown scripts and programs
- Pave the way to standard compliance checking and certification (safety standards, e.g., DO254, ISO26262, etc...)

Achieve **on-the-fly quality monitoring** at **no overhead** to design teams

Capability Highlights

- User-configurable quality checks, metrics, and dashboards
- Monitoring based on user-defined/ vendor-agnostic quality checks, metrics, formulae and verdicts
- Automation based on flexible, flow-aware sensors, easy to edit and maintain
- Scalable product architecture for multi- location usage and dashboard sharing over the net
- Links to text files, user databases, and user scripts or programs
- Interoperability with design tools from most popular EDA vendors, as well as home grown tools and flows
- Hundreds of quality checks and sensors already developed and freely available as templates

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Quality Monitoring

VIP Lane®

Automate your design checklists!

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Where are the bottlenecks?

- Megabytes of data generated every day (log files, user files, doc, SQL DB, ...) means time-consuming analysis
- Manually-filled Excel checklists are tedious and unreliable
- Managers waste 20% to 40% of their time compiling reports
- Concurrent engineering strains efficient communication between teams
- Critical design decisions based on unreliable design data result in high risk
- Home-grown solutions for quality assurance come with high maintenance costs and fast obsolescence

What is the solution?

An enterprise software solution that turns your design practices (IP, SoC, FPGA, software, PCB, embedded system) into reliable quality criteria and metrics and displays dashboards and status reports that are correct by construction.



	Work		Snapshot[1]	
	Count	%	Count	%
Compliant	57	87.69	13	25.49
Not Compliant	8	12.31	36	70.59
Undefined	0	0.0	2	3.92
Error	0	0.0	0	0.0

Section	Work (May 12, 2011)	Snapshot[1]	Action
Design Environment	Reset	Choose	Compute
Front-End Design	RTL	Jan 11th 2011	Compute
SYNTHESIS		Jan 11th 2011	Compute
TIMING			Compute
FED_QC_3.1	Max fan-in	Good (Actual Expected (max) 6 10)	Compute
FED_QC_3.2	Max net capacitance	Good (9)	Compute
FED_QC_3.3	Clock domain table	Bad (15 versus 10 Max)	Compute
		CLK_DDR 256.0MHz	Compute
		CLK_PLL 333.0MHz	Compute
		Clk_ARM 534.0MHz	Compute
		Clk_Osc 172.0MHz	Compute

Check ID	Description	Work (May 12, 2011)	Snapshot[1]	Action
PDS_QC_1.1	Conflict between IP and tool version	Bad (IPName Forbidden version FBCK:IP2 A-2007-12-SP3)	Bad (IPName Forbidden version FBCK:IP2 A-2007-12-SP3)	Compute
PDS_QC_1.2	micos/ptmos Spice version should be 3.0 at least	Good (Version : 3.1)	Good (Version : 3.1)	Compute
PDS_QC_1.3	Tool versions up to date	Good (Design Compiler A-2007-12-SP3 SOC Encounter v09-12-137_1)	Missing info (Design Compiler A-2007-12-SP3 SOC Encounter Not found)	Compute
PDS_QC_1.4	Optimum CPU usage during Back-End	Bad (CPU time 24h 41m 33s Real time 32h 20m 53s)	Unknown (Not Applicable)	Compute
PDS_QC_1.6	All the non-closed bugs are mentioned in the release note	Good	Bad (Missing in RN Bug B0907301507)	Compute

Component	Slack	Action
p	-0.0266	Compute
ip	0.855	Compute
ip	-0.0086	Compute
ip	-0.556	Compute
l_group	-0.063	Compute
core2	0.1844	Compute

“VIP Lane adds new capabilities to the quality design flow that we have been working on for years. These enlarged capabilities lead to **faster identification** of quality metrics requiring special attention, **better communication** between IP and SoC design teams, and measured savings on design time-to-integration.”

– F. Rémond, CAD & Methodology Director, STMicroelectronics